- 2. The borderless contact structure according to claim 1, wherein the etch stop spacer is partially etched.
- 3. The borderless contact structure according to claim 1, wherein the device isolation region comprises a trench isolation region.
- 4. The borderless contact structure according to claim 3, further comprising a thermal oxide layer interposed between the semiconductor substrate and the trench isolation region.
- 5. The borderless contact structure according to claim 4, further comprising a silicon nitride liner interposed between the trench isolation region and the thermal oxide layer.
- 6. The borderless contact structure according to claim 1, wherein the etch stop spacer comprises silicon nitride or silicon oxynitride.
- 7. The borderless contact structure according to claim 1, wherein the etch stop layer comprises silicon nitride or silicon oxynitride.
- 8. The borderless contact structure according to claim 1, further comprising an interconnection line filling the contact hole.
 - 9. The borderless contact structure according to claim 1, further comprising: a contact plug filling the contact hole; and an interconnection line overlying the contact plug.
- 10. The borderless contact structure according to claim 1, wherein the contact hole exposes not only the impurity diffusion region but also a portion of the etch stop spacer adjacent to the exposed impurity diffusion region.